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BT
12-07-01Patent
Attorney's Docket No. 027260-468

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application of

Michio KOMODA et al.

Application No.: 09/879,197

Filed: June 13, 2001

For: DELAY TIME ESTIMATION METHOD
AND RECORDING...

Group Art Unit: 2123

Examiner: Unassigned

RECEIVED

SEP 19 2001

Technology Center 2100

**INFORMATION DISCLOSURE STATEMENT
TRANSMITTAL LETTER**Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

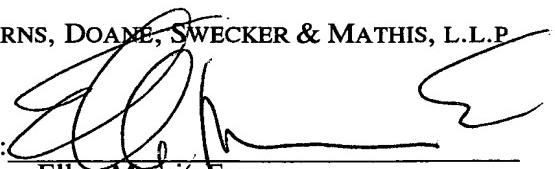
Enclosed is an Information Disclosure Statement and accompanying form PTO-1449 for the above-identified patent application.

- No additional fee for submission of an IDS is required.
- The fee of \$180.00 (126) as set forth in 37 C.F.R. § 1.17(p) is also enclosed.
- A certification under 37 C.F.R. § 1.97(e) is also enclosed.
- A certification under 37 C.F.R. § 1.97(e), and the fee of \$180.00 (126) as set forth in 37 C.F.R. § 1.17(p) are also enclosed.
- Charge \$_____ to Deposit Account No. 02-4800 for the fee due.
- A check in the amount of \$_____ is enclosed for the fee due.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17 and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. This paper is submitted in duplicate.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: 
Ellen Marcie Emas
Registration No. 32,131

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Alexandria, Virginia 22313-1404
(703) 836-6620

Date: September 17, 2001



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INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Date: September 17, 2001

Sir:

In accordance with the duty of disclosure as set forth in 37 C.F.R. § 1.56, Applicant hereby submits the following information in conformance with 37 C.F.R. §§ 1.97 and 1.98. Pursuant to 37 C.F.R. § 1.98, a copy of each of the documents cited is enclosed.

1. "Modeling the Driving-Point Characteristic of Resistive Interconnect for Accurate Delay Estimation", Proc. IEEE International Conference on Computer-Aided Design, 1989.
2. "A Gate-Delay Model for High-Speed CMOS Circuits", Proc. 31st ACM/IEEE Design Automation Conference, 1994.
3. JP-A 9-211087
4. U.S. Application No. 09/878,352, Michio KOMODA et al., June 12, 2001

The documents are being submitted within 3 months of the filing or entry of the national stage of this application or before the first Office Action on the merits, whichever is later, therefore no fee or certification is required under 37 C.F.R. § 1.97(b).

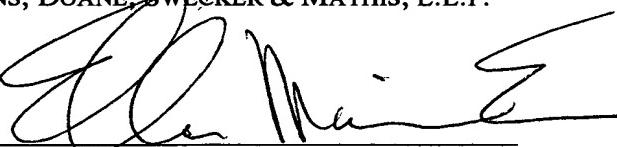
Information Disclosure Statement
Application No. 09/878,352
Attorney's Docket No. 027260-467
Page 2

To assist the Examiner, the documents are listed on the attached form PTO-1449. It is respectfully requested that an Examiner initialed copy of this form be returned to the undersigned.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By:


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Date: September 17, 2001

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

ATTORNEY'S DKT No.
027260-468

APPLICATION No.

APPLICANT

FILING DATE
June 13, 2001

GROUP
2123

SEP 17 2001

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. SEND TO: Assistant Commissioner for Patents, Washington, D.C. 20231.